Comparative Study of Diode Clamped Multilevel Inverter

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Abstract

This paper presents simulation focus in a single phase diode clamped multilevel inverter topology also known as Neutral Point Clamped. Circuit will construct and simulate by using PSIM software and the solution is based on series connection of three to nine-level diode clamped inverters modules. IGBT devices are used almost exclusively in this power range. The more level can be produce, it does will be much better for the application. It is because the value of THD also will decrease once the levels of the multilevel inverter increase. The simulation result shows the total harmonic distortion (THD) for three, five, seven and nine level of diode clamped topologies.

1. Introduction

Concept of the multilevel inverter is same as the other inverter which is to converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits [1]. From the source like batteries, solar panel, wind turbine, or fuel cell the inverter will convert the DC electricity to AC electricity [2]. In this modern technology, Power electronics is very important where it used in a great variety of product. With the high potential in high power for industry, multilevel inverter will become most popular for so many applications.

The developments to use this topology because it's have so many advantages. There have three main features by using multilevel inverter. The most reason is ability to reduce the voltage stress on each power device due to the utilization of multiple levels on the DC bus. Even at low switching frequencies, smaller distortion in the multilevel inverter AC side waveform can be achieved with the step modulation technique. Such as in traction system, when a high DC side voltage is imposed by an application is very important [3].

Multilevel inverters consist in several power semiconductors and capacitor voltage sources. Output voltages of multilevel inverters include the additions of the capacitor voltages due to the commutation of the switches. Figure 1 shows a schematic diagram of one phase leg of inverters with several numbers of levels. The action of power semiconductors is represented by an ideal switch with several actions. A two level inverter, as shown in Figure 1 (a), generates an output voltage of two levels with respect to the negative terminal of the capacitor, while the three-level inverter shown in Figure 1 (b) generates three voltages, and so on. Thus, the output voltages of multilevel inverters have several levels. Moreover, they can reach high voltage, while the power semiconductors must withstand only reduced voltages [4].

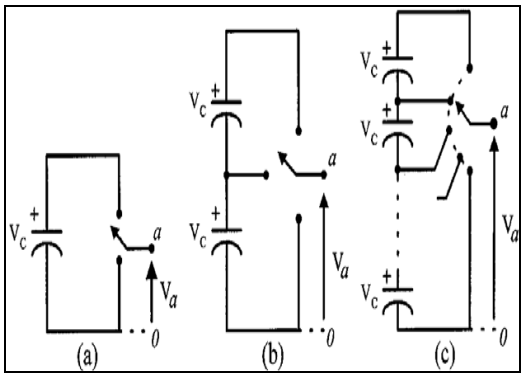

Figure 1: One phase leg of an inverter
(a) Two levels, (b) Three levels, and (c) *n* levels

2. Diode Clamped Topology

The diode clamped inverter more focus on low frequency applications. Also known as Neutral Point Clamped inverter was introduced in early 80's and has been extensively used today in various applications. In early 90's, there have several authors were extended

the concept from three level to multilevel inverter. But there have no reports in practical applications been recorded yet. As shown in Figure 2 is the circuit diagrams for three and five level of diode clamped structure.

Based on concept of using diodes is to limit power devices voltage stress. The output voltage distortion is very low due to multiple levels in the output voltages. The *dv/dt* of switches is low since the switches used to reduced voltage. The switches can operate at a lower switching frequency. In the applications of motor drives, the input currents have low distortions and the common- mode voltages are reduced. The common-mode voltages can be eliminated using sophisticated modulation methods [5].

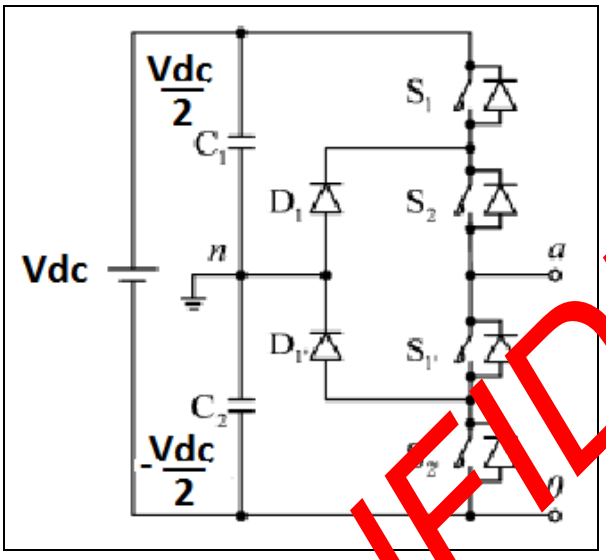

Figure 2: Three Level of diode-clamped multilevel inverter circuit topology

Figure 2 shows the diode clamped of multilevel inverter circuit topologies. The structure and basic principle is consists of series connected capacitors that divide DC bus voltage into a set of capacitor voltages. In Figure 2, it's shown for the three levels diode clamped inverter DC bus is split by two series-connected bank capacitors, C1 and C2. The n can be defined as the neutral point (between two capacitors).

There will be three states for the output voltage which is Vdc/2, 0 and –Vdc/2. These two diode, (D1 and D1') was clamped the switch voltage to half the level of the dc-bus voltage. The sequences when S1 and S2 is turn ON, the voltage across a and 0 is equal with Vdc. In this states, the function of D1' is to balances out the voltage sharing between S1' and S2'. While S1' and S2' blocking the voltage across C1 and C2 to become Vdc/2.

3. Methodology

All procedures are using the same parameter as in Table 1.

Table 1: Input Parameter

Input and Load Parameter	
Input Voltage	360V
Fundamental Frequency	50Hz
Resistance (Load)	100 ohm
Sinusoidal Voltage Source Parameter (Modulation)	
Peak Amplitude	1000V
Modulation Frequency	50Hz
Triangular-wave Voltage Source Parameter (Carrier)	
V Peak to Peak	100V
Carrier Frequency	5KHz

Table 2 show the operation and the characteristic of the switch states for the three-level diode clamped multilevel inverter. Figure 3 shows the schematic circuit for the three level diode clamped multilevel inverter.

Table 2: Three-level diode clamped multilevel inverter voltage levels and corresponding switch state.

Voltage	Switch State			
	S1	S2	S1'	S2'
VDC/2	1	1	0	0
0	0	1	1	0
-VDC/2	0	0	1	1

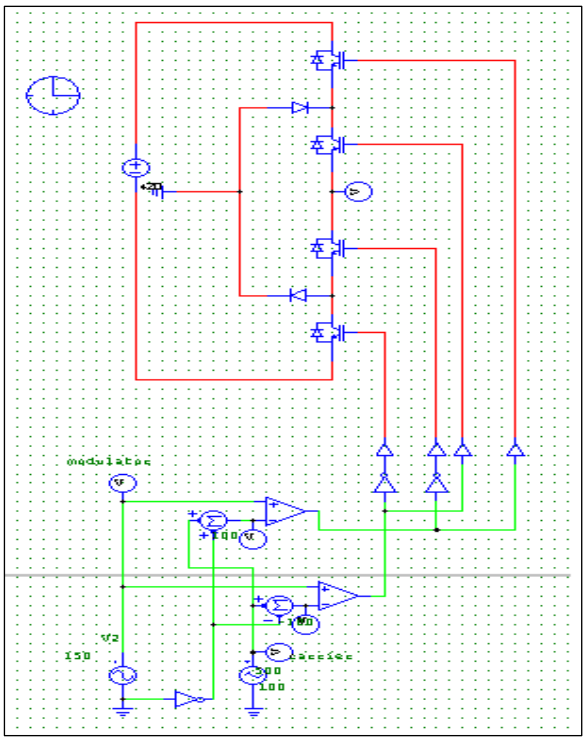

Figure 3: A single-phase three-level diode clamped multilevel inverter circuit.

For control the signal, pulse width modulation (PWM) is the best and easiest technique in controlling the active devices in a multilevel inverter. The PWM method uses several triangle carrier signal and modulation to generate switching signals by comparing between them [6]. Figure 4 shows the basic principle to show the comparison applied to find the output voltage.

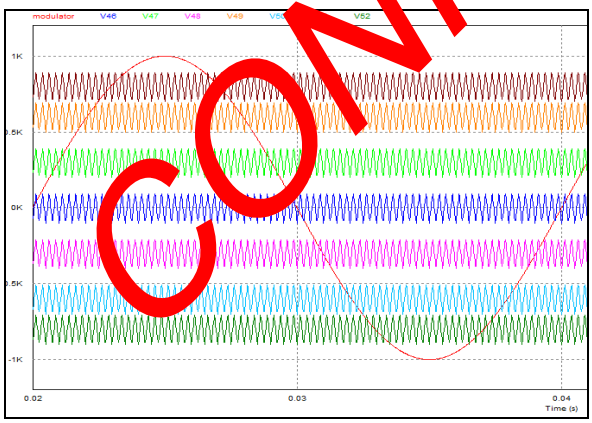

Figure 4: PWM modulation of nine-level DCMLI

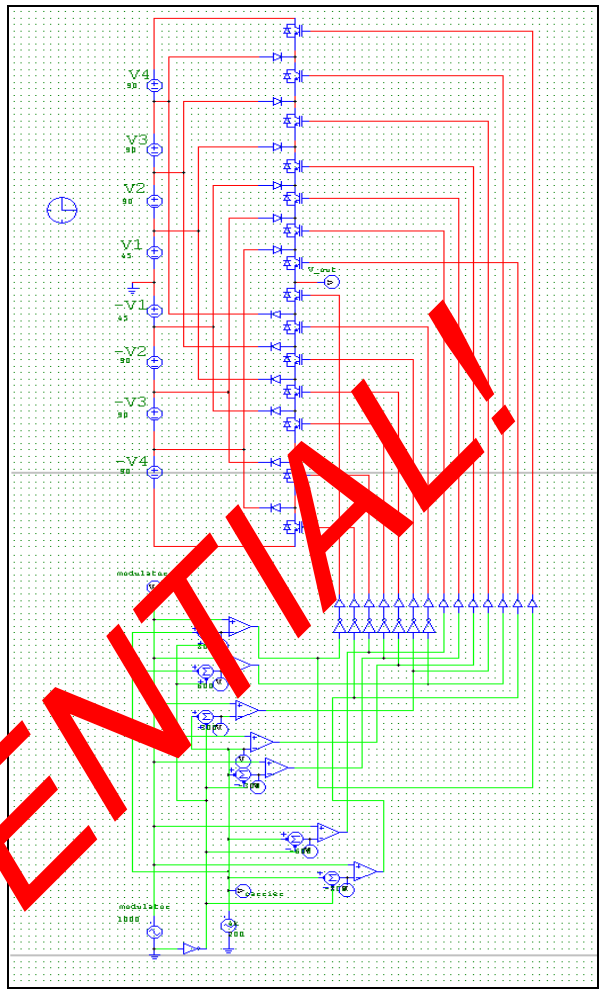

Figure 5: A single-phase nine-level diode clamped multilevel inverter circuit

Referred to the figure 5, it can be seen that each switching device is required to block only a voltage level of Vdc, the clamping diodes required different rating for reverse voltage blocking. For example the last switching state where is when all the switch from S1' to S7' is turn ON, the following diode must block -V1. Same like for the other state. That show about the number of blocking diodes is quadratically relates to the number of levels in a diode clamped topology.

Table 3: Nine-level diode clamped multilevel inverter voltage levels and switch state.

Voltage (V)	Switch State													
	S1	S2	S3	S4	S5	S6	S7	S1′	S2′	S3′	S4′	S5′	S6′	S7′
V1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
V2	0	1	1	1	1	1	1	1	0	0	0	0	0	0
V3	0	0	1	1	1	1	1	1	1	0	0	0	0	0
V4	0	0	0	1	1	1	1	1	1	1	0	0	0	0
-V4	0	0	0	0	1	1	1	1	1	1	1	0	0	0
-V3	0	0	0	0	0	1	1	1	1	1	1	1	0	0
-V2	0	0	0	0	0	0	1	1	1	1	1	1	1	0
-V1	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Table 3 shows the nine-level diode clamped multilevel inverter voltage levels and switching state for the circuit diagram in Figure 5. The sequences could be elaborate such as:

For voltage level Van = V1, turn on all upper switches S1 ~ S7.

For voltage level Van = V2, turn on upper switches S2 ~ S7 and lower switch S1'.

For voltage level Van = V3, turn on upper switches S3 ~ S7 and lower switches S1' and S2'.

For voltage level Van = V4, turn on upper switches S4 ~ S7 and lower switches S1' ~ S3'.

For voltage level Van = -V4, turn on upper switches S5 ~ S7 and lower switches S1' ~ S4'.

For voltage level Van = -V3, turn on upper switches S6 ~ S7 and lower switches S1' ~ S5'.

For voltage level Van = -V2, turn on upper switch S7 and lower switches S1'~ S6'.

For voltage level Van = -V1, turn on all lower switches S1'~ S7'.

4. Result and Discussion

Figure 6 shows the output voltage of the single phase nine-level diode clamped multilevel inverter by using PWM method. To control the circuit, Pulse-width modulation (PWM) is a commonly technique to use for controlling power in electrical devices and it made practical by modern electronic power switches [7].

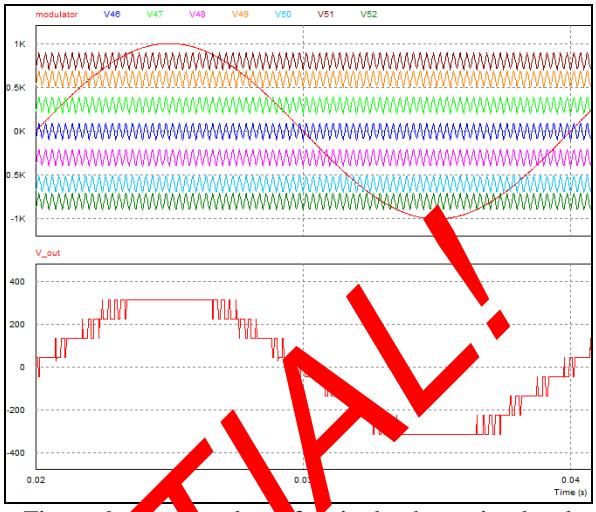

Figure 6: Output voltage for single phase nine-level diode clamped

PWM switching frequency has to be much faster than would affect the load, which is to say the device that uses the power. Figure 7. This is a simple method to generate the PWM pulse train corresponding to a given signal is the interceptive PWM: the signal (modulation) is compared with a saw tooth waveform (carrier). When the latter is less than the former, the PWM signal (VP1) is in high state (1). Otherwise it is in the low state (0).

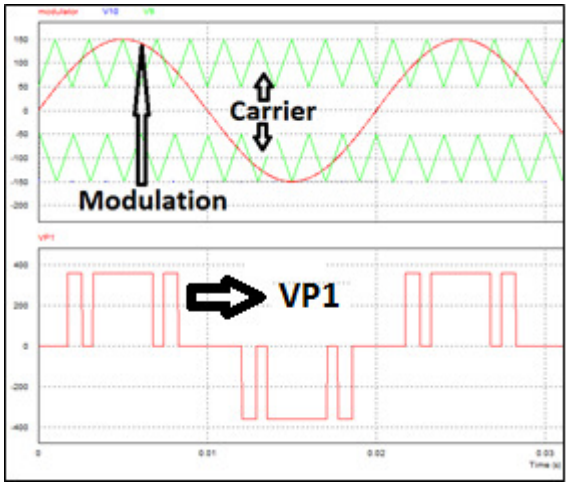

Figure 7: Output voltage for single phase three-level diode clamped

In Figure 8 and 9 below show the Total Harmonic Distortion (THD) spectrum for the output voltage in each level. Based on the simulation result its shows

there have very low THD level when increased the level of multilevel inverter [8].

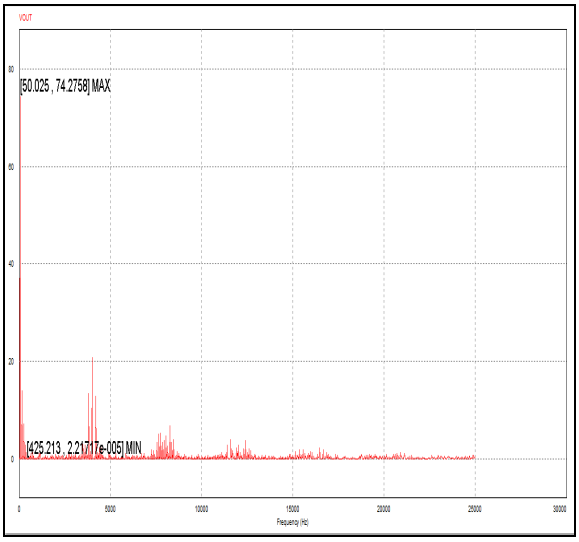

Figure 8: THD spectrum for the output voltage for three level circuits

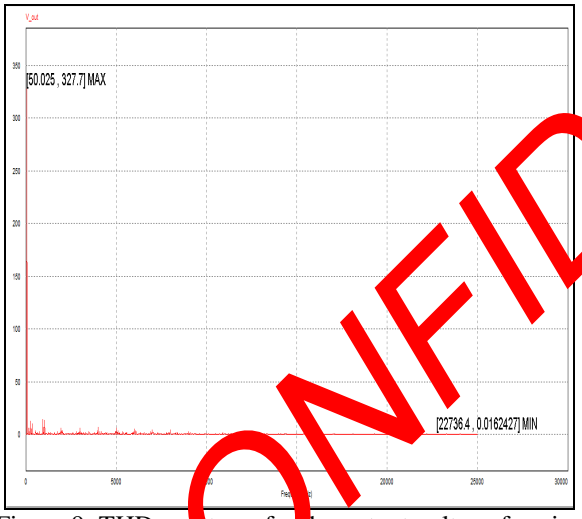

Figure 9: THD spectrum for the output voltage for nine level circuits.

This proved as more levels can be formed, there was less THD happened. It's shown as in Table 4.

Table 4: Comparison level by THD and Current (Load)

Stage of Multilevel	THD (%)	Current (A) (LOAD)
3 Level	118.00	30.00
5 Level	31.27	15.42
7 Level	19.70	3.60
9 Level	11.30	3.15

When increased levels of the inverter then indirectly help to reduce the THD and can improve the performance of the application. FFT or Fast Furrier Transform was applied to the output voltage to get the THD result.

5. Conclusion

As a conclusion, this paper focused about the single-phase diode-camped multilevel inverter. It was achieved the expected result by simulated the diode clamped topology with different level to compared the THD result. The circuit was designed with the PSIM software package where is easiest to use PWM method to get the result. This topology not only to reduce the harmonics distortions but can be used on the low frequency application such as in motor drives [9].

6. References

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